Listing of Claims:

1. (Presently Amended) A Global Positioning System (GPS) receiver comprising:

a first section having a signal acquisition stage for acquiring an input signal and a sampling stage for sampling the input signal at a sampling data rate to provide sampled data; and

a second section having an I/O data buffer for receiving and buffering the sampled data and providing the buffered data to tracker hardware, wherein the tracker hardware operates at an operational rate which is greater than the sampling data rate of the input signal enabling multiple cycling of the buffered data by the I/O data buffer,

wherein the tracker hardware is single channel receiver hardware behaving as multi-channel receiver hardware

wherein the tracker hardware includes a plurality of Field Programmable Gate Arrays for operating the tracker hardware at the operational rate,

further comprising a first processor for at least performing navigation functions and controlling the tracker hardware, and a second processor for at least performing tracking functions, wherein the first and second processors are interfaced by interface hardware.

2. (Cancelled)

3. (Cancelled)

4. (Originally Presented) The GPS receiver according to Claim 1, wherein the sampling data rate is approximately 2 MHz and the operational rate is approximately 50 MHz.

5. (Cancelled)

6. (Presently Amended) The GPS receiver according to Claim 1, wherein the interface hardware is a dual-port memory.

7. (Presently Amended) The GPS receiver according to Claim 1, further comprising an external interface connected to the first processor for at least uploading software to the first processor.

8. (Presently Amended) The GPS receiver according to Claim 1, wherein the second processor provides data associated with a tracking state vector to the tracker hardware

and controls the I/O data buffer to stream at least a portion of the sampled data to the tracker hardware for processing.

9. (Originally Presented) The GPS receiver according to Claim 8, wherein the second processor processes data outputted by the tracker hardware from processing a previous data stream while the tracker hardware processes the at least the portion of the sampled data.

10. (Presently Amended) The GPS receiver according to Claim 1, wherein the tracking and navigation functions are performed simultaneously.

11. (Originally Presented) The GPS receiver according to Claim 1, wherein the sampled data provided by the first section includes Inphase and Quadrature sampled data, and wherein the first section further provides a sampling clock to the second section.

12. (Originally Presented) The GPS receiver according to Claim 1, wherein the I/O data buffer provides the sampled data to the tracker hardware in batches to provide for batch-mode processing of the sampled data.

13. (Originally Presented) The GPS receiver according to Claim 1, wherein the signal acquisition stage includes a down-converter filter and a Low Noise Amplifier (LNA) connected to an antenna for acquiring the input signal.

14-18. (Cancelled)

19. (Originally Presented) A Global Positioning System (GPS) receiver comprising:

a first section having a signal acquisition stage for acquiring an input signal and a sampling stage for sampling the input signal at a sampling data rate to provide sampled data; and

a second section having an I/O data buffer for receiving and buffering the sampled data and providing the buffered data to tracker hardware in batches to be processed by the tracker hardware by batch-mode processing.

20. (Originally Presented) The GPS receiver according to Claim 19, wherein the tracker hardware is single channel receiver hardware behaving as multi-channel receiver hardware.

21. (Originally Presented) The GPS receiver according to Claim 19, wherein the tracker hardware includes a plurality of Field Programmable Gate Arrays.

22. (Originally Presented) The GPS receiver according to Claim 19, wherein the sampling data rate is approximately 2 MHz, and wherein an operational rate of the tracker hardware is approximately 50 MHz.

23. (Originally Presented) The GPS receiver according to Claim 19, further comprising a first processor for at least performing navigation functions and controlling the tracker hardware, and a second processor for at least performing tracking functions.

24. (Originally Presented) The GPS receiver according to Claim 23, wherein the second processor provides data associated with a tracking state vector to the tracker hardware and controls the I/O data buffer to stream at least a portion of the sampled data to the tracker hardware for processing.

25. (Originally Presented) The GPS receiver according to Claim 24, wherein the second processor processes data outputted by the tracker hardware from processing a previous data stream while the tracker hardware processes the at least the portion of the sampled data.

26. (Originally Presented) The GPS receiver according to Claim 23, wherein the tracking and navigation functions are performed simultaneously.

27. (Originally Presented) The GPS receiver according to Claim 19, wherein the sampled data provided by the first section includes Inphase and Quadrature sampled data, and wherein the first section further provides a sampling clock to the second section.

28. (Originally Presented) The GPS receiver according to Claim 19, wherein the signal acquisition stage includes a down-converter filter and a Low Noise Amplifier (LNA) connected to an antenna for acquiring the input signal.

29. (Originally Presented) A method for processing an input signal received by a Global Positioning System (GPS) receiver, the method comprising the steps of:

sampling the input signal at a sampling data rate to provide sampled data;

buffering the sampled data by a data buffer; and

providing the buffered data to tracker hardware in batches to be processed by the tracker hardware by batch-mode processing.

30. (Originally Presented) The method according to Claim 29, wherein the tracker hardware is single channel receiver hardware behaving as multi-channel receiver hardware.

31. (Originally Presented) The method according to Claim 29, wherein the tracker hardware includes a plurality of Field Programmable Gate Arrays.

32. (Originally Presented) The method according to Claim 29, wherein the sampling data rate is approximately 2 MHz, and wherein an operational rate of the tracker hardware is approximately 50 MHz.

REMARKS/ARGUMENTS

Applicant respectfully traverses Examiner's rejection of claims 1, 4, 6-13 under 35 U.S.C. 102 (b) which have been amended to place these claims in order for allowance along with claims 19-32.

CONCLUSION

On the basis of the above amendments and remarks, reconsideration and allowance of this application is believed warranted. If the Examiner believes, for any reason, that personal communication will expedite prosecution, the Examiner is invited to telephone the undersigned at the number provided.

THE JOHNS HOPKINS UNIVERSITY
Applied Physics Laboratory

By BY Y.R
Benjamin Y Roca
Reg. No. 50,166
Tel.: (240) 228-5644

BYR/lh